AMENDMENTS TO THE CLAIMS

The following listing of claims replaces all prior versions and listings of claims in the above-referenced application:

1. (Canceled)

2. (Currently amended) An integrated circuit, comprising:

a scan path having an input and an output;

an input/output (I/O) [~~a~~] pin coupled to the input and the output of the scan path, wherein the I/O pin inputs scan test data to the scan path at a first test time responsive to an input enable control signal; and

wherein the I/O pin outputs scan test data from the scan path at a second test time.

3. (Previously presented) An integrated circuit, comprising:

a first scan path;

a second scan path;

a first I/O pin inputting input scan test data to an input of the first scan path at a first test time and outputting output scan test data from an output of the second scan path at a second test time responsive to a first input enable control signal; and

a second I/O pin inputting input scan test data to an input of the second scan path at the first test time and outputting output scan test data from an output of the first scan path at the second test time responsive to a second input enable control signal.

4. (Previously presented) The integrated circuit of claim 3, wherein at least one of the first scan path and the second scan path further comprises a series of scan paths.

5. (Previously presented) The integrated circuit of claim 2, wherein the scan path comprises a series of scan paths.

6. (Previously presented) The integrated circuit of claim 2, further comprising functional circuitry, wherein the scan path interacts with the functional circuitry.

7. (Currently amended) The integrated circuit of claim 2, further comprising functional circuitry, wherein:

the ~~first~~ I/O pin inputs functional test data to the functional circuitry at a third test time; and

the ~~first~~ I/O pin outputs functional test data from the functional circuitry responsive to an output enable control signal at a fourth test time.

8.-11. (Canceled)

12. (Currently amended) An integrated circuit, comprising:

a functional circuit producing functional output;

an I/O pin that acts as an input at a first time and as an output at a second time, the I/O pin having a respective scan path that produces scan output;

an I/O circuitry, comprising:

an input buffer responsive to an input enable control signal and coupled to (1) the I/O pin to receive an input signal and to (2) ~~to~~ the functional circuit to provide the input signal;

a virtual pin output buffer responsive to a virtual pin enable control signal coupled to the I/O pin to provide output; ~~and~~

a virtual pin multiplexer coupled to (1) the functional circuit to receive the functional output and (2) the scan path to receive the scan output, the virtual pin multiplexer providing a virtual pin multiplexer output; and

a virtual pin flip-flop coupled to (1) the virtual pin multiplexer to receive the virtual pin multiplexer output, the virtual pin flip-flop holding the received data for a clock cycle.

13. (Previously presented) The integrated circuit of claim 12, further comprising:

a number of scan paths;

the same number of I/O pins; and

the same number of I/O circuitries, wherein the same number of virtual pin flip-flops forms at least one register.

14. (Previously presented) The integrated circuit of claim 13, wherein:

each virtual pin flip-flop further comprises:

a compact control signal;

an output data signal; and

an and-gate receiving the compact-control signal and the output-data signal to eliminate don't-care data; and

the register is a compaction register.

15. (Previously presented) The integrated circuit of claim 13, wherein:

each I/O circuitry further comprises:

a reseed multiplexer receiving (1) the scan output from the scan path and (2) scan input derived from the input buffer, the reseed multiplexer providing the scan output or the scan input to the virtual pin multiplexer; and

a reseed control signal controlling the reseed multiplexer; and the register is a reseed register.

16. (Previously presented) The integrated circuit of claim 13, wherein:

each I/O circuitry further comprises:

an XOR-gate coupled to receive a linear feedback shift register (LFSR) input and a LFSR feedback, the XOR-gate providing an XOR-gate output;

a reseed multiplexer coupled to receive (1) the XOR-gate output and (2) scan input, the reseed multiplexer providing a reseed multiplexer output;

a reseed flip-flop coupled to receive the reseed multiplexer output, the reseed flip-flop providing a reseed flip-flop output; and

an input multiplexer coupled to receive the input signal and the reseed flip-flop output, the input multiplexer generating the scan input.

17. (Previously presented) The integrated circuit of claim 13, further comprising a second number of flip-flops that form a compaction register, wherein:

the integrated circuit performs reseeding and compaction at the same time.

18. (Previously presented) The integrated circuit of claim 17, wherein the compaction register is read serially.

19. (Currently amended) A method, comprising:

inputting scan data to an I/O pin during a first time;

processing the scan data in a respective scan path to produce scan output data in response to an input enable control signal and a mode control signal; and

outputting scan output data to the I/O pin at a second time in response to an output enable control signal.

20. (Previously presented) The method of claim 19, further comprising:

multiplexing output data and scan output data; and

storing the output data or the scan output data in a flip-flop during the first time.

21. (Previously presented) The method of claim 20, further comprising:

connecting a number of flip-flops associated with I/O pins; and

forming a register for performing a reseed test.

22. (Previously presented) The method of claim 21, wherein forming a register further comprises:

sending a compact control signal;

and-gating the compact control signal with the output data;

eliminating the don't care data; and

performing compaction.

23. (Previously presented) The method of claim 21, wherein forming a register further comprises:

sending a reseed control signal to a reseed multiplexer;

multiplexing functional output data and scan input data; and

performing the reseed test.

24. (Previously presented) The method of claim 23, wherein multiplexing further comprises:

receiving gated input from a linear feedback shift register; and

performing a linear feedback shift register reseed test.

25. (Previously presented) The method of claim 19, wherein the first time and the second time occur during the same clock cycle.

26. (Previously presented) The integrated circuit of claim 12 further comprising:

an output buffer coupled to (1) the functional circuit to receive the functional output and (2) the I/O pin to provide the functional output.